Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method for debugging a computer system, comprising:

initiating a process in the computer system, the process including instructions and running on a processor in the computer system;

launching a debugger program that is embedded in a ROM of the computer system, the debugger program running on the processor;

executing at least part of the instructions by the processor; and

the debugger program operating on at least part of the executed instructions.

Claim 2 (Original): A method as defined in claim 1, further comprising:

the debugger program capturing a trace of the at least part of the executed instructions.

Claim 3 (Original): A method as defined in claim 2 wherein:

the computer system includes a port connected to a monitoring system;

and further comprising:

outputting the captured trace through the port to the monitoring system.

Claim 4 (Original): A method as defined in claim 1, wherein:

the process comprises a boot process;

the instructions comprise boot instructions stored in the ROM of the computer system; and

the debugger program is launched from within the boot process.

Claim 5 (Original): A method as defined in claim 1, further comprising:

stopping the execution of the instructions at a first break point;

the debugger program setting a second break point in the instructions; and

continuing the execution of the instructions.

Claim 6 (Original): A method as defined in claim 5, further comprising:

the debugger program disassembling a current instruction of the instructions;

determining a length of the current instruction, the length of the current instruction indicating a start point for a next instruction of the instructions; and

setting the second break point at the start point of the next instruction.

Claim 7 (Original): A method as defined in claim 1, further comprising:

interrupting the execution of the instructions at a current instruction;

the debugger program operating on the current instruction by disassembling the current instruction; and

executing the current instruction.

Claim 8 (Original): A method as defined in claim 7, further comprising:

before executing the current instruction, determining a location of a next instruction of the instructions; and

after executing the current instruction, interrupting the execution of the instructions at the next instruction.

Claim 9 (Original): A method as defined in claim 1, further comprising:

setting a switch within the computer system; and

launching the debugger program in response to detecting the set switch.

Claim 10 (Original): A method as defined in claim 1, further comprising:

setting a break point within the process according to a location specified in a map of the process contained in the debugger program.

Claim 11 (Currently Amended): A computer system, comprising:

at least one processor;

a read-only memory (ROM) connected to the processor;

a target process having instructions, executable ~~capable of being executed~~ by the processor; and

a debugger program embedded within the ROM, executable by the processor, ~~and capable of being executed by the processor~~ to operate on at least part of the instructions of the target process.

Claim 12 (Original): A computer system as defined in claim 11, wherein:

the target process comprises a boot process.

Claim 13 (Original): A computer system as defined in claim 11, wherein:

the debugger program operates on the at least part of the instructions by capturing a trace of the execution of the at least part of the instructions.

Claim 14 (Original): A computer system as defined in claim 11, wherein:

the debugger program further operates on the at least part of the instructions by disassembling the at least part of the instructions.

Claim 15 (Original): A computer system as defined in claim 11, wherein:

the debugger program operates on a current instruction of the target process and sets a break point at a next instruction of the target process to be operated on.

Claim 16 (Original): A computer system as defined in claim 11, further comprising:

a switch that when set enables launching of the debugger program;

and wherein the target process launches the debugger program upon detecting that the switch is set.

Claim 17 (Original): A computer system as defined in claim 11, further comprising:

an interrupt flag that when set causes an interruption of execution of the target process;

and wherein, upon interruption of the execution of the target process, the debugger program operates on a current instruction of the target process.

Claim 18 (Original): A computer system as defined in claim 11, further comprising:

a map of the target process embedded in the debugger program and specifying locations of parts of the target process.

Claim 19 (Currently Amended): A computer debugging system, comprising:

a target computer;

a monitoring system connected to the target computer;

a data storage device in the monitoring system;

a read-only memory (ROM) in the target computer;

a processor in the target computer;

a target process having instructions executable by the processor in the target computer; and

a debugger program embedded in the ROM and executable by the processor in the target computer to generate data on the execution of at least part of the instructions of the target process and to transfer the data to the monitoring system for recording in the data storage device.

Claim 20 (Original): A computer debugging system as defined in claim 19, further comprising:

a disassembler embedded in the ROM and executable in the target computer to disassemble the at least part of the instructions of the target process.

Claim 21 (Original): A computer debugging system as defined in claim 19, wherein:

the data on the execution of the at least part of the instructions of the target process comprises a trace capture of the at least part of the instructions.

Claim 22 (Currently Amended): A computer system, comprising:

a read-only memory (ROM) means for storing computer control instructions;

a means for executing a target process;

a ROM-embedded means for interrupting the execution of the target process at a current instruction, the interrupting means being executable by the target process executing means;

a ROM-embedded means for disassembling the current instruction, the disassembling means being executable by the target process executing means;

a means for executing the current instruction; and

a ROM-embedded means for capturing a trace of the current instruction and of results of the execution of the current instruction, the trace capturing means being executable by the target process executing means.

Claim 23 (Original): A computer system as defined in claim 22, further comprising:

a means for transferring the captured trace to an external means for storing the captured trace.

Claim 24 (Currently Amended): A computer system comprising:

a processor;

a read-only memory (ROM);

a target process having executable instructions that are executable by the processor; and

a debugger program embedded within the ROM and having a disassembler and a trace capturer that are executable by the processor;

and wherein:

the debugger program interrupts execution of the target process at some of the instructions;

the disassembler disassembles at least some of the instructions at which the execution of the target process is interrupted; and

the trace capturer captures a trace of at least some of the disassembled instructions.

Claim 25 (Original): A computer system as defined in claim 24, wherein:

the target process comprises a boot process stored within the ROM and having instructions that boot the computer system when the boot process executes.

Claim 26 (Original): A computer system as defined in claim 24, further comprising:

a port that can be connected to a monitoring system;

and wherein the debugger program outputs the captured trace through the port to the monitoring system.

Claim 27 (Original): A computer system as defined in claim 24, wherein:

the debugger program disassembles a current instruction of the target process, determines a length of the current instruction, and sets a break point at a next instruction of the target process.

Claim 28 (Original): A computer system as defined in claim 24, wherein:

the computer system executes the current instruction, encounters the break point at the next instruction, and jumps to the debugger program with the next instruction as a new current instruction.

Claim 29 (Currently Amended): A computer system comprising:

a switch;

a processor;

a target process having executable instructions that are executable by the processor; and

a debugger program that is executable by the processor;

and wherein:

when the switch is off, the debugger program cannot be launched in the processor; and

when the switch is on, the debugger program can be launched in the processor to interrupt execution of the target process in the processor at some of the

instructions and operate on at least some of the instructions at which the execution of the target process is interrupted.

Claim 30 (Currently Amended): A method for debugging a target process executing on a computer system, comprising:

launching, in a processor of the computer system, a debugger program from a read-only memory (ROM) of the computer system, the ROM having a boot process and the debugger program embedded therein, the debugger program having a disassembler and a trace capturer;

interrupting execution, in the processor, of the target process at an instruction;

the disassembler disassembling, in the processor, the instruction; and

the trace capturer capturing a trace, in the processor, of the instruction.

Claim 31 (Original): A method as defined in claim 30, further comprising:

executing the instruction; and

interrupting the execution of the target process after the instruction.

Claim 32 (Original): A method as defined in claim 30, wherein:

the target process comprises the boot process.

Claim 33 (Currently Amended): A method for debugging a target process executing on a computer system, comprising:

setting a switch within the computer system to one of an on state and an off state;

when the switch is set to the off state, preventing execution of a debugger program in a processor of the computer system; and

when the switch is set to the on state:

launching the debugger program in the processor;

interrupting, in the processor, execution of the target process at an instruction; and

the debugger program operating, in the processor, on the instruction.